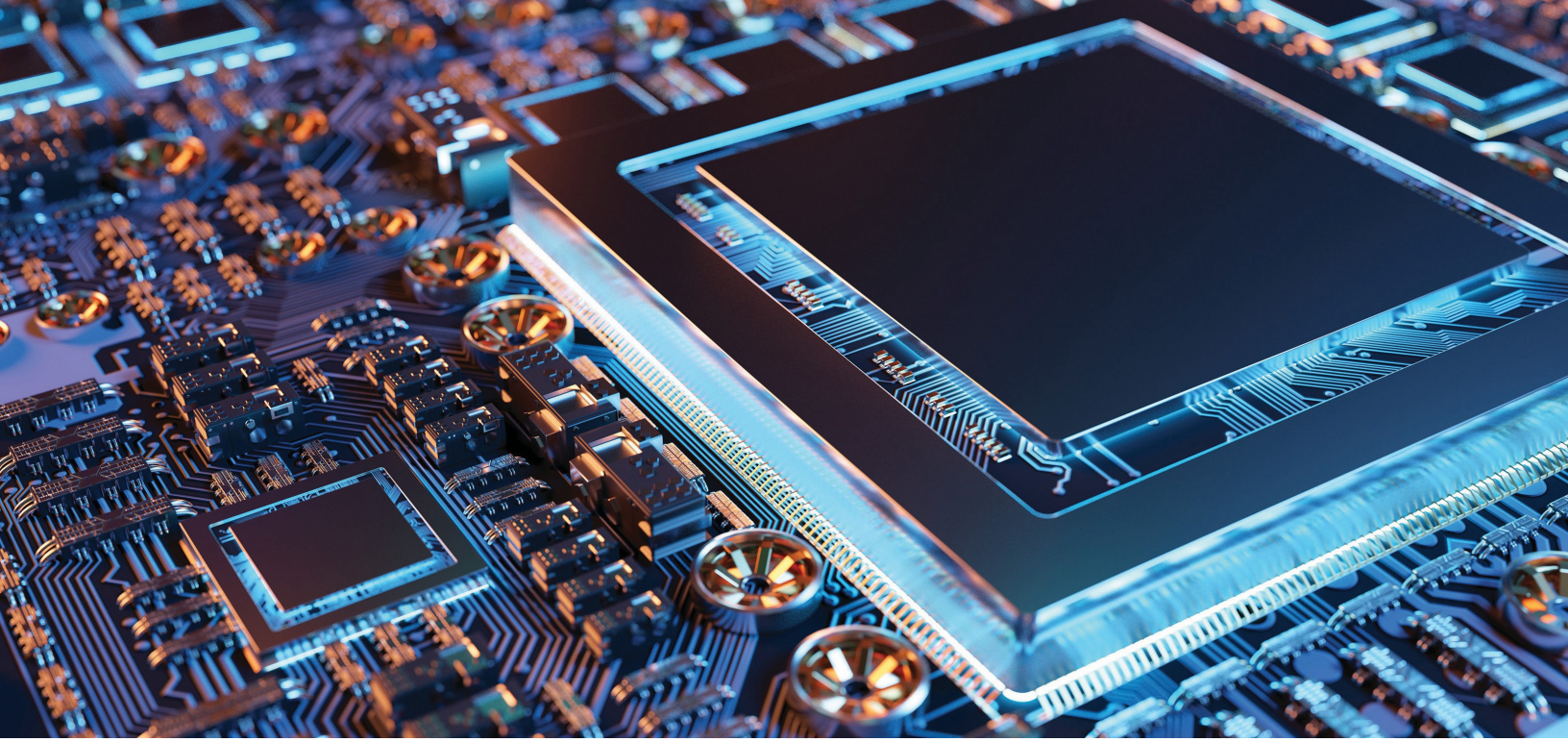
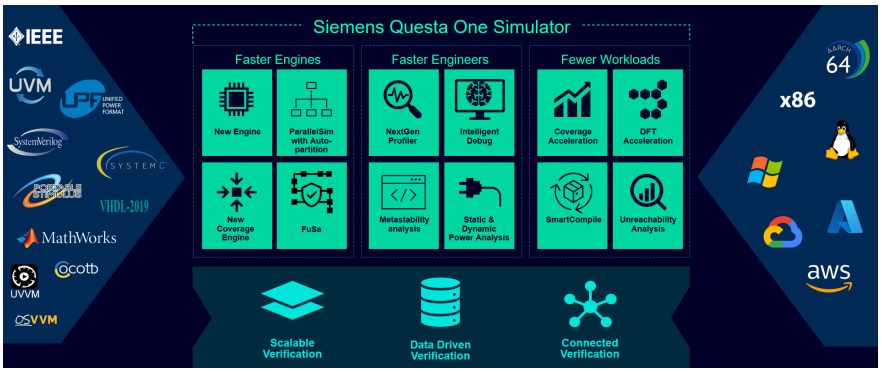


DIGITAL INDUSTRIES SOFTWARE

Questa One Sim

Benefits

- Industry-leading, high-performance, multi-language simulator
- Fastest simulator for design-for-test (DFT) pattern verification
- High-performance, high-capacity integrated debug environment
- Coverage acceleration for faster coverage closure
- SmartCompile and multi-core simulations for overall performance boost
- Universal Verification Methodology (UVM), SystemVerilog, VHDL, SystemC, and mixed language support
- Integrated Portable Stimulus Standard (PSS) engine
- Reference simulator for LRM compatibility



Sophisticated SoC verification

Questa One Sim software from Siemens EDA, a part of Siemens Digital Industries Software, is a purpose-built simulator that addresses the growing complexity of ASIC, SoC, and FPGA designs. In addition to the sheer size of designs and the inclusion of multiple embedded processors and advanced interconnect systems, the increase in software content and the configurability required by multi-platform design requires a functional verification solution that unifies a broad arsenal of verification features. As well, time-to-market pressures dominate verification projects. To deliver quality on schedule requires shortening the time to achieve coverage and quality goals and necessitates improved debug productivity.

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Benefits *continued*

- Native compiled, single kernel simulator technology
- Code coverage and functional coverage
- SystemVerilog Assertion (SVA) and Property Specification Language (PSL) support
- Simulate in advanced optimization mode
- Profiling for hotspot analysis
- C code debug
- X-propagation dynamic simulation
- Native integration with Questa One Sim Xact
- Real number modeling
- CDC metastability injection in simulation
- Best-in-class, power-aware verification technology
- Common coverage database and flows
- 64-bit support for Linux and Windows

Platform support

- Windows 11 (both 32 bit and 64 bit)
- Linux – x86 - RHEL 8 and 9, Rocky 8 and 9, SLES 15 SP4 (both 32 bit and 64 bit)
- Linux – AARM64 RHEL 8 and 9, Rocky 8 and 9

Questa One Sim's powerful new technologies help maximize the effectiveness of verification at the block and subsystem levels, improving overall productivity. Questa One Sim achieves industry-leading performance and capacity through very aggressive, global compile and simulation optimization algorithms for SystemVerilog, VHDL and SystemC.

With its unique SmartCompile capabilities, Questa One Sim supports very fast turnaround times and effective library management. Questa One Sim maintains high performance using ParallelSim, while its integrated debug environment provides high-performance, high-capacity debugging, thus enabling dramatic regression throughput improvements when running a large suite of tests.

Advanced verification methodologies

Design verification is a complex and sophisticated process. To provide best-in-class capabilities to address the toughest verification challenges, Questa One Sim supports a wide range of advanced verification methodologies, including the latest UVM standard for verification. Design completeness is measured through code and functional coverage, which include statement, expression, condition, toggle and finite state machine coverage.

Assertion-based verification (ABV) improves design quality through the insertion of white-box monitors that allow active monitoring of functional correctness within the debugger window. Questa One Sim enables ABV through support of SVA constructs and the PSL. It also offers powerful debug capabilities with the assertion thread viewer.

Questa Portable Stimulus (QPS) is a particularly powerful enhancement to Questa One Sim. QPS supports the Accellera PSS, enabling engineers to create abstract, reusable test intent that can be automatically translated into multiple verification environments, including UVM sequences for simulation and C code for embedded software testing.

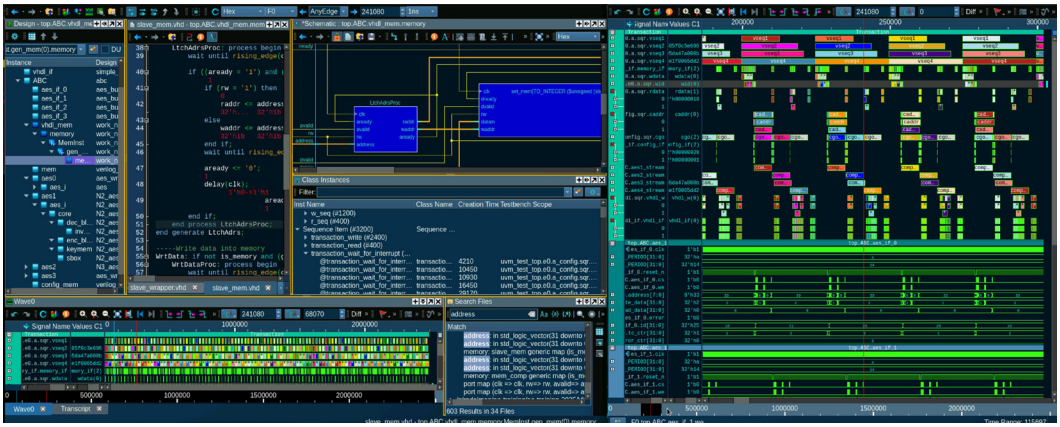
Questa One Sim also integrates VHDL into its industry-best constraint solver, allowing it to generate more complex VHDL constrained random stimulus. It also enables the ability to save the VHDL functional coverage data into the Unified Coverage Data Base format, offering VHDL verification as a native part of Questa One Sim. UVM already incorporates these new features to enhance the already popular VHDL verification methodology.

Accelerate simulation performance with ParallelSim

On top of high-performance optimizations, Questa One Sim accelerates simulations even further by running them on multiple cores with the ParallelSim capability, which allows for easy-to-use auto-partitioning that determines the best number of partitions to achieve optimal performance. The in-built qualifier determines the design fit, which gives the flexibility to enable ParallelSim on only designs that are suitable for parallelization.

Next generation integrated debug

Questa One Sim is a context-aware, integrated simulation and debug platform that supports complete logic verification flows. It has intuitive features with powerful design and verification debug capabilities for debugging in live-sim mode or post-sim mode. Questa One Sim's high-performance, high-capacity debugger quickly finds RTL, gate-level and protocol bugs. It has various advanced debug windows tailored for UVM testbenches. It is SystemVerilog class-based and UVM-aware to speed up overall debug time, even on today's most complex SoCs and FPGAs. New capabilities such as constraints debug, X-debug and protocol debug make it a versatile tool for verification engineers. Low-power and UPF debug is fully integrated and overlaid with RTL views.



New performance profiling capabilities

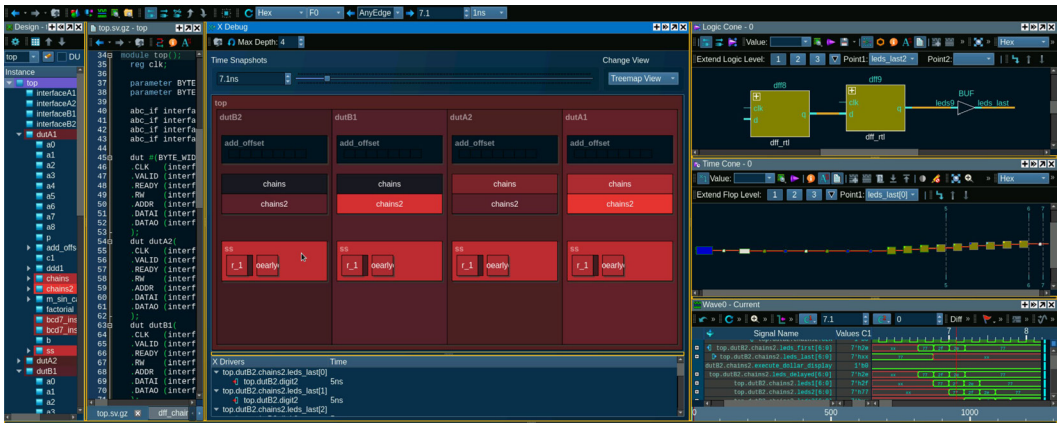
Maximizing the efficiency of RTL verification often requires analyzing simulation run-time performance to look for bottlenecks and potential improvements. Questa One Sim's new, completely re-architected and intuitive performance profiler helps users self-diagnose performance bottlenecks by highlighting inefficiencies in the design or testbench that are sub-optimal and can be fixed. The new enhanced capability enables profiling across a single test, across multiple-tests, or even an entire regression.

Optimized flow using qrun with SmartCompile

Questa One Sim supports advanced optimization algorithms designed to significantly improve simulation performance. To improve compilation, optimization and elaboration turn-around times, Questa One Sim supports a single compile command wrapper, called qrun, which uses SmartCompile capabilities that automatically provide incremental compile — the ability to save and reuse pre-compiled parts as preoptimized design units (PDUs) and save and reuse elaboration images. These features can be used individually or in combination to provide customized flows that reduce turnaround times by removing unneeded reprocessing.

X-Propagation

One of the major challenges in simulation is X-propagation. Determining the sources of propagated Xs requires greater debug time late in the verification cycle, as engineers must identify the sources of Xs, test the initialization of the design, and create explicit checks to report Xs. Questa One Sim's Xprop enabled dynamic simulation consists of mechanisms to handle the propagation of Xs. It ensures simulation closely matches silicon behavior, traps the source of Xs during simulation, and ensures signals resolve to a known value if possible. Combine these features with the all-new X-Debug capability and heat maps to get a Questa One Sim debugger that allows for a much more efficient way of debugging Xs.



Real number modeling

Questa One Sim supports real number modeling. Real number modeling enables better modeling of analog blocks and allows these discrete models to be used in high-performance digital flows.

Expand with other Questa One Sim technologies

Questa One Sim Power Aware (Questa One Sim PA) enables early low power verification of active power management at the RTL, even for the most complex designs. This ensures that the power management architecture and behavior are correct and that the design will operate correctly during active power management. Based on the latest industry standard IEEE 1801, Questa One Sim PA supports the latest UPF 4.0 and all of UPF 3.1/3.0/2.1/2.0 specifications for active power management

Achieving coverage closure in modern SystemVerilog UVM environments remains a costly and time-consuming process. Questa One Sim Coverage Acceleration (Questa One Sim CX) is a coverage acceleration capability that uses innovative technologies to help users start coverage early, ramp up faster and close coverage more predictably.

Questa One Sim DFT Acceleration (Questa One Sim DX), in conjunction with Tessent Silicon Lifecycle, offers an all-encompassing solution that delivers the productivity and performance benefits required to sign-off ATPG and MBIST pattern verification.

Questa One Sim Xact (Sim Xact) enables much quicker gate-level simulation bring-up by automatically eliminating pesky false Xs, zero-delay race conditions, and library modeling errors, while isolating hard to diagnose connectivity problems. Plus, Sim Xact supports advanced real X root cause tracing tools.

Questa One Sim Fault Acceleration (Questa One Sim FX) for functional safety is a high-performance fault simulator for mitigating random hardware faults, ensuring the reliability and safety of automotive systems. Questa One Sim FX verifies if a design meets stringent fault injection requirements specified in the ISO 26262 automotive safety standard.

Questa One Sim FX for DFT is a high-performance simulator used in DFT for functional fault grading to enhance defect coverage of complex ICs. Integration with market-leading Tessent TestKompress offers a powerful solution for approaching zero defective parts per million.

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